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these devices to obtain the desired  
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CTS is the process of connecting the

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Automation: Navrood A. Sherwani

clocks to all clock pin of sequential circuits by using inverters/ buffers in order to balance the skew and to minimize the insertion delay. All the clock pins are driven by a single clock source. Clock balancing is important for meeting all the design constraints.

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Automation covers all aspects of physical  
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physical design cycle. In addition, newer topics like physical design automation of FPGAs and MCMs have been included.

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The course will introduce the participants

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to the basic design flow in VLSI physical design automation, the basic data structures and algorithms used for implementing the same. The course will also provide examples and assignments to help the participants to understand the concepts involved, and appreciate the main challenges therein.

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