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Circuits offers a modern, up-to-date look at computer-aided design (CAD) of very large-scale integration (VLSI) circuits. In particular, this book covers techniques for synthesis and optimization of digital circuits at the architectural and logic levels, i.e., the generation of performance-and/or area-optimal circuits representations from models in hardware description ...

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In this introductory paper to the field, it is our goal to provide a new unified look at synthesis problems that is independent from the level of

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abstraction like system, RTL, and logic (for refinements targeted to hardware), or process- and basic block level (for refinements targeted to software). For each level of our model called " double roof " , synthesis requires the solution of three basic problems, namely allocation (of resources), binding, and scheduling Based on the " double roof ...

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Topics covered include hardware modeling, compilation techniques for hardware models, high-level

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Circuits, logic synthesis, and library mapping algorithms. Course titles include Digital CAD, Advanced Logic Design or Complements of VLSI Design.

Synthesis and Optimization of Digital
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Combinational logic optimization is traditionally divided into two-level and multiple-level logic synthesis. Two-level synthesis targets the realization of combinational logic functions by a two-layer interconnection of elementary logic gates, such as AND-OR, NAND-NAND, etc.

SYNTHESIS AND OPTIMIZATION OF SYNCHRONOUS LOGIC CIRCUITS

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In particular, this book covers
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0-07-016333-2. (NB. Chapters 7–9

cover combinatorial two-level, combinatorial multi-level, and

respectively sequential circuit

optimization.) Hachtel, Gary D.;

Somenzi, Fabio (2006) [1996]. Logic

Synthesis and Verification Algorithms.

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This new graduate textbook in computer engineering offers a modern, up-to-date look at computer aided design of VLSI circuits at the functional and logic level by addressing an interesting topic in CAD for digital circuits: design synthesis of detailed specifications from abstract models. Topics covered include hardware modeling, compilation techniques for hardware models, high-level synthesis, logic synthesis, and library mapping algorithms. Course titles include Digital CAD, Advanced Logic Design or Complements of VLSI Design.

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Logic Synthesis and Optimization presents up-to-date research information in a pedagogical form. The authors are recognized as the leading experts on the subject. The focus of the book is on logic minimization and includes such topics as two-level minimization, multi-level minimization, application of binary decision diagrams, delay optimization, asynchronous circuits, spectral method for logic design, field programmable gate array (FPGA) design, EXOR logic synthesis and technology mapping. Examples and illustrations are included so that each contribution can be read independently. Logic Synthesis and Optimization is an indispensable reference for academic researchers as well as professional CAD engineers.

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Synthesis and Optimization of DSP Algorithms describes approaches taken to synthesising structural hardware descriptions of digital circuits from high-level descriptions of Digital Signal Processing (DSP) algorithms. The book contains: -A tutorial on the subjects of digital design and architectural synthesis, intended for DSP engineers, -A tutorial on the subject of DSP, intended for digital designers, -A discussion of techniques for estimating the peak values likely to occur in a DSP system, thus enabling an appropriate signal scaling. Analytic techniques, simulation techniques, and hybrids are discussed. The applicability of different analytic approaches to different types of DSP design is covered, -The development

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Of techniques to optimise the precision requirements of a DSP algorithm, aiming for efficient implementation in a custom parallel processor. The idea is to trade-off numerical accuracy for area or power-consumption advantages. Again, both analytic and simulation techniques for estimating numerical accuracy are described and contrasted. Optimum and heuristic approaches to precision optimisation are discussed, -A discussion of the importance of the scheduling, allocation, and binding problems, and development of techniques to automate these processes with reference to a precision-optimized algorithm, -Future perspectives for synthesis and optimization of DSP algorithms.

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Circuits is composed of two parts. The first part introduces the concepts of the design of digital systems using contemporary field-programmable gate arrays (FPGAs). Various design techniques are discussed and illustrated by examples. The operation and effectiveness of these techniques is demonstrated through experiments that use relatively cheap prototyping boards that are widely available. The book begins with easily understandable introductory sections, continues with commonly used digital circuits, and then gradually extends to more advanced topics. The advanced topics include novel techniques where parallelism is applied extensively. These techniques involve not only core reconfigurable logical elements, but also use embedded blocks such as memories

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Circuits and digital signal processing slices and interactions with general-purpose and application-specific computing systems. Fully synthesizable specifications are provided in a hardware-description language (VHDL) and are ready to be tested and incorporated in engineering designs. A number of practical applications are discussed from areas such as data processing and vector-based computations (e.g. Hamming weight counters/comparators). The second part of the book covers the more theoretical aspects of finite state machine synthesis with the main objective of reducing basic FPGA resources, minimizing delays and achieving greater optimization of circuits and systems.

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Finite State Machine-Datapath

Design, Optimization, and

Implementation explores the design space of combined FSM/Datapath implementations. The lecture starts by examining performance issues in digital systems such as clock skew and its effect on setup and hold time constraints, and the use of pipelining for increasing system clock frequency. This is followed by definitions for latency and throughput, with associated resource tradeoffs explored in detail through the use of dataflow graphs and scheduling tables applied to examples taken from digital signal processing applications. Also, design issues relating to functionality, interfacing, and performance for different types of memories commonly found in ASICs and FPGAs such as FIFOs, single-

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Circuits

ports, dual-ports, and register files are examined. Finally, design issues regarding cooperating Finite State Machine/Datapaths are explored. All design examples are presented in implementation-neutral Verilog code and block diagrams, with associated design files available as downloads for both Altera Quartus and Xilinx Virtex FPGA platforms. A working knowledge of Verilog, logic synthesis, and basic digital design techniques is required. This lecture is suitable as a companion to the synthesis lecture titled Introduction to Logic Synthesis using Verilog HDL.

Logic Synthesis and Verification Algorithms is a textbook designed for courses on VLSI Logic Synthesis and Verification, Design Automation, CAD and advanced level discrete

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mathematics. It also serves as a basic reference work in design automation for both professionals and students. Logic Synthesis and Verification Algorithms is about the theoretical underpinnings of VLSI (Very Large Scale Integrated Circuits). It combines and integrates modern developments in logic synthesis and formal verification with the more traditional matter of Switching and Finite Automata Theory. The book also provides background material on Boolean algebra and discrete mathematics. A unique feature of this text is the large collection of solved problems. Throughout the text the algorithms covered are the subject of one or more problems based on the use of available synthesis programs.

Revised, and updated Design and

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Optimization in Organic Synthesis presents strategies to explore experimental conditions and methodologies for systematic studies of entire reaction systems (substrates, reagent(s), catalyst(s), and solvents). Chemical phenomena are not usually the result of a single factor and this book describes how statistically designed methods can be used to analyse and evaluate synthetic procedures. The methodology is based on multivariate statistical techniques. The accompanying CD contains data tables and programmes. This book is essential reading for anyone working in process design and development in fine chemicals or the pharmaceutical industry, and is suitable for those with no experience in the field. *

Contains recalculated models and

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redrawn figures, as well as new chapters on for example, the design of combinatorial libraries * Presents strategies to explore experimental conditions and methodologies * Enables the analysis and prediction of the best synthetic procedures

Introduction to Logic Synthesis Using Verilog HDL explains how to write accurate Verilog descriptions of digital systems that can be synthesized into digital system netlists with desirable characteristics. The book contains numerous Verilog examples that begin with simple combinational networks and progress to synchronous sequential logic systems. Common pitfalls in the development of synthesizable Verilog HDL are also discussed along with methods for avoiding them. The

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Circuits target audience is anyone with a basic understanding of digital logic principles who wishes to learn how to model digital systems in the Verilog HDL in a manner that also allows for automatic synthesis. A wide range of readers, from hobbyists and undergraduate students to seasoned professionals, will find this a compelling and approachable work. The book provides concise coverage of the material and includes many examples, enabling readers to quickly generate high-quality synthesizable Verilog models.

This book presents the hardware implementation of control algorithms represented by graph-schemes of algorithm. It includes new methods of logic synthesis and optimization for logic circuits of Mealy and Moore

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